AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (original) A semiconductor integrated circuit device comprising:

(a) a first memory array area which includes a plurality of first memory cells and first data lines which are formed on a first layer and connected with said first memory cells;

(b) a second memory array area which includes a plurality of second memory cells and second data lines which are formed on said first layer and connected with said second memory cells;

(c) a sense amplifier area which includes sense amplifiers;

(d) a first connecting area located between said first memory array area and said sense amplifier area; and

(e) a second connecting area located between said second memory array area and said sense amplifier area,

wherein said semiconductor integrated circuit device further includes:

(f) first lines which are formed on a second layer different from said first layer and connected with said first data lines in said first connecting area; and

(g) second lines which are formed on said second layer and connected with said second data lines in said second connecting area,

said sense amplifiers being connected between said first lines and said second lines and adapted to amplify voltage differences between said first lines and said second lines.

2. (original) A semiconductor integrated circuit device according to claim 1, wherein said first memory array area, said first connecting area, said sense amplifier area, said second connecting area, and said second memory array area are located to align in this order in the extending direction of said first and second data lines.

3. (original) A semiconductor integrated circuit device according to claim 1, wherein said first memory array area, said first connecting area, said sense amplifier area, said second connecting area, and said second memory array area are areas having virtually rectangular shapes,

wherein said semiconductor integrated circuit device further includes a switch forming area which is located between said first memory array area and said first connecting area,

wherein said switch forming area includes data transfer lines (IO) and switch circuits having signal transfer paths which are connected between said first data lines and said data transfer lines, said data transfer lines being formed on said second layer to extend in a direction which intersects said first lines.

4. (original) A semiconductor integrated circuit device according to claim 2, wherein said first and second lines are laid out over said sense amplifier area.

5. (original) A semiconductor integrated circuit device according to claim 2, wherein at least part of said first and second lines are laid out over said sense amplifier area.

6. (original) A semiconductor integrated circuit device according to claim 2, wherein said second layer is an upper layer relative to said first layer.

7. (original) A semiconductor integrated circuit device according to claim 2, wherein said first and second lines are formed to extend in the extending direction of said first and second data lines.

8. (original) A semiconductor integrated circuit device according to claim 1 further including word lines which intersect said first and second data lines at right angles, said memory cells being formed at all intersections of said first and second data lines and said word lines and each made up of a data transfer MISFET and a capacitor, with the gate electrode of said MISFET being connected to a word line.

9. (original) A semiconductor integrated circuit device according to claim 1, wherein said first lines, second lines, first data lines and second data lines are formed by use of a Levenson's line-and-space mask which is coated with shifters of alternately different phases.

10. (original) A semiconductor integrated circuit device according to claim 1, wherein said first and second data lines have a virtually equal line spacing.

11. (original) A semiconductor integrated circuit device according to claim 1, wherein said first and second lines and said first and second data lines have a line spacing which is equal to a minimum working dimension.

12. (original) A semiconductor integrated circuit device according to claim 1, wherein said memory cells are each formed in an area having a size of $4F^2$ (where F denotes a minimum working dimension).

Claims 13-26 (cancelled)